REMARKS

Applicants wish to thank the Examiner for the courtesies extended to the undersigned during the telephone interview. An Interview Summary is submitted herewith.

Applicants hereby add new claim 37. Accordingly, claims 1-13, 15-27, and 30-37 are pending in the present application.

Claims 1, 3-13, 15-17, 19-22, 27, 30, 32, 34, and 36 stand rejected under 35 USC 102(b) for anticipation by U.S. Patent No. 4,794,441 to Sugawara. Claim 2 and 14 stand rejected under 35 USC 103(a) for obviousness by U.S. Patent No. 4,175,240 to Kremlev. Claim 18 stands rejected under 35 USC 103(a) for obviousness over Sugawara in view of U.S. Patent No. 5,652,183 to Fujii. Claims 23-26, and 28 stand rejected under 35 USC 103(a) for obviousness over Kalinsky. Claims 29, 31, 33, and 35 stand rejected under 35 USC 103(a) for obviousness in view of U.S. Patent No. 5,608,616 to Umeda.

Applicants respectfully traverse the rejections and urge allowance of the present application.

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. See, e.g., MPEP §2143 (8th ed.).

Claim 1 has been amended to recite limitations of claim 29 reciting the 5,000, or

more, field effect transistors coupled in parallel to form the power semiconductor switching device. Sugawara discloses two FETs G1 and G2 coupled in parallel to control operation of npn transistor 9 as set forth in the teachings of col. 7, lines 48-63. The Examiner states on page 5 of the Office Action that it would have been obvious to use 5000 or more transistors since the applicants have not disclosed that this cut-off number serves a specific purpose and it appears the device performs equally well with a different number of transistors. Applicants disagree.

As discussed during the interview, transistors 10, 11 of Sugawara merely provide control of the operation of npn transistor 9. There is no teaching or suggestion of forming transistors 10, 11 to form a power semiconductor switching device comprising 5,000 or more transistors, especially since transistors 10, 11 do not conduct power currents but merely operate to control the operation of transistor 9. Further, numerous issues are raised by the utilization of 5,000 or more transistors coupled in parallel which are not addressed by the prior art. For instance, gate capacitance issues are raised which impacts the switching operations of the transistors as well as issues regarding the one resistance (Ron). The statement that Applicants have not disclosed the cut-off number serves a specific purpose is mistaken. Applicants refer the Examiner to the teachings of the specification at least at pages 37-38 wherein Applicants state numerous transistors are utilized to form the power semiconductor switching device to operably conduct power currents. Limitations of claim 1 are not shown nor suggested by the prior art and claim 1 is allowable for at least this reason.

Further, there is no motivation to modify the teachings of Sugawara. Referring to MPEP §2143.01 (8th ed.), there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify or combine reference teachings. The mere fact that references *can* be combined or modified does not render the resultant combination obvious *unless the prior art also suggests the desirability of the combination*. MPEP §2143.01 *citing In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990). Obviousness cannot be established by a combination of references unless there is some motivation in the art to support the combination. *See ACH Hospital Systems, Inc. v. Montifiore Hospital*, 732 F.2d 1572, 1577, 221 USPQ 929, 933 (Fed. Cir. 1984). The motivation for forming the combination must be something other than hindsight reconstruction based on using Applicant's invention as a road map for such a combination. *See, e.g., Interconnect Planning Corp. v. Feil*, 227 USPQ 543, 551 (Fed. Cir. 1985); *In re Mills*, 16 USPQ2d 1430 (Fed. Cir. 1990).

There is no teaching in the art that the device of Sugawara is defective or provides deficient operation to motivate one of ordinary skill in the art to look for additional reference teachings to replicate transistors 10, 11 by an order of thousands as claimed. The transistors 10, 11 operate as control transistors and accordingly there is no motivation to provide additional transistors to provide a power semiconductor switching device as claimed. There is no motivation to modify the reference teachings of Sugawara in support of the rejection of claim 1 including the limitations of claim 29 and claim 1 is allowable for at least this additional reason.

The claims which depend from independent claim 1 are in condition for allowance for the reasons discussed above with respect to the independent claim as well as for their own respective features which are neither shown nor suggested by the cited art.

Claim 12 has been amended using limitations of claim 28 to define that the forming the power field effect transistor comprises configuring the power field effect transistor to operably conduct currents in excess of 1 Ampere. As discussed during the interview, transistors 10, 11 of Sugawara provide control operations and npn transistor 9 is the main drive section. There is absolutely no teaching to provide control transistors 10, 11 configured to operably conduct power currents in excess of 1 Ampere as claimed. Further, the Office Action relied upon teachings of Sugawara and Kalinsky to support the rejection of previously pending claim 28. However, the Office Action fails to identify any reference teachings disclosing or suggesting a field effect transistor comprising a plurality of planar field effect transistors electrically coupled in parallel and configured to operably conduct power currents in excess of 1 Ampere. Limitations of claim 12 are not shown nor suggested by the prior art and claim 12 is allowable for this additional reason.

Further, there is no motivation to support the combination of reference teachings. It is stated on page 4 of the Action that the combination is appropriate to enable further *control* of current between the two nodes. However, claim 12 now recites the planar field effect transistors of the power field effect transistor conduct power currents in excess of 1 Ampere. There is no motivation to provide the claimed power field effect transistor as claimed and claim 12 is allowable for this additional reason.

The claims which depend from independent claim 12 are in condition for allowance for the reasons discussed above with respect to the independent claim as well as for their own respective features which are neither shown nor suggested by the cited art.

New claim 37 recites the field effect transistors comprise only n-channel devices as previously recited in claim 31. It is stated on pages 4-5 of the Office Action that it would have been obvious to use the n-channel transistors of Umeda because n-channel transistors are faster than p-channel transistors. Applicants disagree.

Sugawara specifically discloses the use of transistor 10 comprising a p-channel device and transistor 11 comprising an n-channel device as set forth in col. 7, lines 22-32. Col. 7, lines 48-63 provides explicit teachings regarding the specific utilization of the n-channel and p-channel devices to provide at least one conducting device in the presence of different voltage conditions. Accordingly, there is no suggestion to modify the reference teachings to comprise only n-channel devices as claimed. Claim 37 is allowable.

Further, the modification of Sugawara as alleged in the Office Action would destroy the purpose of Sugawara and the 103 rejection of new claim 37 is improper for at least this additional reason. *In re Fitch*, 972 F.2d 1260, 1265 n.12, 23 USPQ2d 1780, 1783 n.12 (Fed. Cir. 1992) (stating that a proposed modification is inappropriate for an obviousness inquiry when the modification renders the prior art inoperable for its intended purpose).

Moreover, there is no motivation to modify the Sugawara teachings as alleged in the Office Action. There is no motivation to provide faster devices and the specific teachings of col. 7, lines 48-62 teach away from the proposed modification. There is no motivation

and the 103 rejection is improper for this additional reason.

Applicants include copies of previously field Information Disclosure Statements and accompanying 1449 forms which have not been initialed by the Examiner. Applicants respectfully request initialization of the 1449 forms and return of the forms to Applicants.

Applicants request allowance of all pending claims.

The Examiner is requested to phone the undersigned if the Examiner believes such would facilitate prosecution of the present application. The undersigned is available for telephone consultation at any time during normal business hours (Pacific Time Zone).

Respectfully submitted,

Dated: 9/10/03

By: _____
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